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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/786,388	03/02/2001	Erwin Thurner	P01.0041	8156

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/786,388	THURNER, ERWIN	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/2/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been examined and claims 1-14 have been rejected.

Priority

2. Acknowledgment is made of Applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy of the priority document for PCT/DE99/02753, filed on September 1, 1999, has been received in this National Stage application from the International Bureau. The priority date is September 2, 1998.

Drawings

3. The drawings are objected to for the following reasons. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3-1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

(a) "the representation component 200", as described in line 17 of page 7.

(b) "The screen surface 200", as described in line 18 of page 7.

Specification

4. The disclosure is objected to because of the following informalities:

Appropriate correction is required.

4-1. It appears that "a further step of checing the graphic structure", as described in lines 22-23 of page 4, should be "a further step of checking the graphic structure".

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6-1. Claim 1 recites the limitation "said selected graph structure file" in step c) of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim examination, the Examiner will presume that "said selected graph structure file" as described in claim 1 refers to "said selected graphic structure file".

6-2. Claim 6 recites the limitation "said set of graph structure files" in step b) of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim examination, the Examiner will presume that "said set of graph structure files" as described in claim 6 refers to "said set of graphic structure files".

6-3. Claim 7 recites the limitation "the graph" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

6-4. Claim 12 recites the limitation "said structure of a technical system" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of

claim examination, the Examiner will presume that "said structure of a technical system" as described in claim 12 refers to "said graphic structure of a technical system".

6-5. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-10 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cantone et al., U.S. Patent 5,594,657 issued January 14, 1997, in view of Nishi et al., "Engineering Modeler: A CASE Tool Building Support Environment for System Development", Savemation Review, Vol. 15, No. 1, February, 1997, pages 68-74.

8-1. Regarding claim 1, Cantone et al. disclose a method for determining a graphic structure of a technical system, comprising the steps of:

b) selecting said elements (design elements, column 16, lines 17-23) in said graphic structure file in such a way that said technical system is described using said selected elements (the element to be added is selected, column 16, lines 50-67), and

c) representing said elements by an editor program into which said selected graphic structure file has been integrated, which determines said graphic structure of said technical

system (The selected design element will appear in the canvas area, column 16, lines 50-67; FIG. 6).

Cantone et al. fail to expressly disclose selecting a graphic structure file from a set of a plurality of different graphic structure files.

Nishi et al. disclose an engineering modeler that supports the environment where the development of various systems design support software tools may be performed. Furthermore, Nishi et al. disclose an object oriented framework for CASE tool development and an implementation framework common to CASE tools for various types of system development support (Nishi, page 1). The configuration of an engineering modeler is shown in Figure 1 including a plurality of libraries in the object component repository. Specifically, Nishi et al. disclose the missing element:

a) selecting a graphic structure file from a set of a plurality of different graphic structure files (Nishi, program diagrams, section 3.1, paragraph 1, page 10), each graphic structure file containing indications of which elements can be selected to represent it in order to describe the structure of the technical system graphically (Nishi, providing system constituent unit object components and enabling design editing visually with program diagrams, section 3.1, paragraph 1, page 10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Cantone et al. to incorporate the teachings of Nishi et al. to obtain the invention as specified in claim 1 because it will provide an implementation framework common to CASE tools for various types of system development support (Nishi, page 1).

8-2. Regarding claim 2, Cantone et al. further disclose said technical system is an electronic circuit (In describing circuits, users may use a graphics tool, column 1, line 62 through column 2, line 6).

8-3. Regarding claim 3, Cantone et al. further disclose said technical system is a piece of technical equipment (FPGA chip, column 2, lines 7-14).

8-4. Regarding claim 4, Cantone et al. further disclose said elements are graphic elements of a graphic which describe said technical system (icons representing design elements, column 16, lines 17-23).

8-5. Regarding claim 5, Nishi et al. disclose comprising the step of checking said graphic structure of said technical system for predefined structure rules (Nishi, Complete check function, line 5 of Figure 2, page 4).

8-6. Regarding claim 6, Cantone et al. disclose an arrangement (graphics tool, column 16, lines 7, through column 18, line 47) for determining a graphic structure of a technical system, comprising:

c) a processor configured to execute an editor program (window type editor, column 16, lines 11-13), said editor program being used to determine a graphic with elements of said selected graphic structure file (design elements, column 16, lines 17-23) via which a graphic structure is determined (FIG. 6); and

d) a representation component which is coupled to said editor program and with which a specific graphic structure can be represented (graphical display screen, column 16, lines 11-13).

Cantone et al. fail to expressly disclose (a) a memory in which a set of a plurality of different graphic structure files are stored, each said graphic structure file comprising indications

of which elements can be selected to represent it in order to form a graphic, and (b) a selector unit with which a graphic structure file can be selected from said set of graph structure files.

Nishi et al. disclose an engineering modeler that supports the environment where the development of various systems design support software tools may be performed. Furthermore, Nishi et al. disclose an object oriented framework for CASE tool development and an implementation framework common to CASE tools for various types of system development support (Nishi, page 1). The configuration of an engineering modeler is shown in Figure 1 including a plurality of libraries in the object component repository. Specifically, Nishi et al. disclose the missing elements:

a) a memory in which a set of a plurality of different graphic structure files are stored, each said graphic structure file comprising indications of which elements can be selected to represent it in order to form a graphic (Nishi, Object component repository, Key:8 of Figure 1, page 3);

b) a selector unit with which a graphic structure file can be selected from said set of graphic structure files (Nishi, Library (L), Key:2 of Figure 3(b), page 6);

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Cantone et al. to incorporate the teachings of Nishi et al. to obtain the invention as specified in claim 6 because it will provide an implementation framework common to CASE tools for various types of system development support (Nishi, page 1).

8-7. Regarding claim 7, Cantone et al. further disclose a structure of a technical system is described using the graph (FIG. 6).

8-8. Regarding claim 8, Cantone et al. further disclose said technical system is an electronic circuit (In describing circuits, users may use a graphics tool, column 1, line 62 through column 2, line 6).

8-9. Regarding claim 9, Cantone et al. further disclose said technical system is a piece of technical equipment (FPGA chip, column 2, lines 7-14).

8-10. Regarding claim 10, Cantone et al. and Nishi et al. further disclose comprising:

a) a first subarrangement which comprises said memory (Nishi, Object component repository, Key:8 of Figure 1, page 3); and

b) a second subarrangement which is coupled to said first subarrangement and comprises:

said selector unit (Nishi, Library (L), Key:2 of Figure 3(b), page 6);

said editor program (The graphics tool displays a window type editor, column 16, lines 11-13); and

said representation component (graphical display screen, column 16, lines 11-13).

8-11. Regarding claim 12, Cantone et al. further disclose said graphic structure of a technical system is described using a graphic (FIG. 6).

8-12. Regarding claim 13, Cantone et al. further disclose said technical system is an electronic circuit (In describing circuits, users may use a graphics tool, column 1, line 62 through column 2, line 6).

8-13. Regarding claim 14, Cantone et al. further disclose said technical system is a piece of technical equipment (FPGA chip, column 2, lines 7-14).

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Cantone et al., U.S. Patent 5,594,657 issued January 14, 1997, and Nishi et al.,

"Engineering Modeler: A CASE Tool Building Support Environment for System Development", Savemation Review, Vol. 15, No. 1, February, 1997, pages 68-74, as applied to claim 10 and further in view of Burrows et al., U.S. Patent 6,397,117 B1 issued May 28, 2002, and filed May 28, 1998.

9-1. Regarding claim 11, Cantone et al. disclose a method for determining a graphic structure of a technical system. Neither Cantone et al. nor Nishi et al. expressly disclose said first subarrangement and said second subarrangement are coupled to one another via a communications network. Nevertheless, Cantone et al. suggest the invented FPGA synthesis system relates generally to computer aided design (CAD) of electronic circuits (column 1, lines 11-12) because its output can be used by other lower level CAD tools for placement and routing (column 2, lines 10-14).

Burrows et al. disclose a distributed computer aided design system as shown in FIG. 2. A server station communicates with the plurality of client stations via a communications medium, which is preferably an intranet or internet medium. One of its advantages is that the file storage for the CAD tool executables and libraries is only necessary at the server station, and only the master copy of this needs to be backed up. Users are therefore relieved of the requirement to maintain the CAD tool executables and libraries (Burrows, column 2, lines 34-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined teachings of Cantone et al. and Nishi et al. to incorporate the teachings of Burrows et al. to obtain the invention as specified in claim 11 because users will be relieved of the requirement to maintain the CAD tool executables and libraries (Burrows, column 2, lines 34-38).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. Reference to Fukasawa et al., U.S. Patent 5,367,468 issued November 22, 1994, is cited as disclosing a design aid method for integrated circuits.

Reference to Batch et al., U.S. Patent 5,423,023 issued June 6, 1995, is cited as disclosing a user configurable system which integrates and manages a plurality of different tasks and software tools.

Reference to Pillans, U.S. Patent 5,644,728 issued July 1, 1997, is cited as disclosing a control system including a visual interface representing and allowing editing of subimages and links.

Reference to Berg et al., U.S. Patent 5,999,911 issued December 7, 1999, and filed June 2, 1995, is cited as disclosing a method for managing workflow.

Reference to Egilsson, U.S. Patent 6,286,017 B1 issued September 4, 2001, and filed August 1, 1996, is cited as disclosing a graphical environment for managing and developing applications.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The Examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jean Homere can be reached on (703) 308-6647. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day H.D.
October 17, 2004

JEAN R. HOMERE
PRIMARY EXAMINER